Digital modulator using digitally programmable Complementary metal–oxide–semiconductor Differential Voltage Current Conveyor

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Abstract

This study aims to Developing a digital modulation system using a new technology and idea, which is the digitally programmable CMOS (Complementary metal–oxide–semiconductor), Integrate the CMOS DVCC circuit as a modulator in the communication systems, as will be explained in chapter 3, Finally, simulate this new idea in communication by using a simulation program, which is PSpice software, and analyzing the results. By focusing on How to use digital programmable CMOS (Complementary Metal–Oxide–Semiconductor) in a communication system as a digital modulator, Verifying the effectiveness of the study using simulation software such as PSpice and MATLAB, and Analyzing and verifying the effectiveness of the three modified modulation techniques. Digitally programmable Binary Amplitude shift keying (DP BASK), Digitally programmable Binary Phase shift keying (DP BPSK), And Digitally programmable Binary Frequency shift keying (DP BFSK).

This study adopts an applied research approach. The study demonstrated that the CMOS DVCC circuit could be successfully integrated into communication systems as a digital modulator. The study recommended to conduct further research on the noise resistance capabilities of the DP modulation techniques, and explore additional modulation techniques that could benefit from digitally programmable CMOS technology, such as Quadrature Amplitude Modulation (QAM) or Orthogonal Frequency-Division Multiplexing (OFDM).

Keywords: Digital modulator, digitally programmable, Complementary metal–oxide–semiconductor, Differential Voltage, Current Conveyor

1. Introduction:

The integration of digitally programmable Complementary Metal–Oxide–Semiconductor (CMOS) technology with Differential Voltage Current Conveyor (DVCC) circuits represents a significant advancement in digital modulation techniques. Digital modulators are essential in modern communication systems, enabling efficient signal transmission by modulating carrier signals based on input data. The use of CMOS DVCC circuits allows for greater flexibility and precision in controlling the modulation process, enhancing the performance of digital communication systems (Gandewar et al., 2016; Ferri et al., 2022). This study focuses on developing and simulating a digital modulator utilizing this innovative technology to improve the efficiency of digital modulation methods like ASK, FSK, and PSK.

1.1 Modulation

Modulation is a common practice in communication systems where a very high-frequency carrier wave is used to transmit a low-frequency message signal, preserving all the information present in the original message signal. And the carrier signal is a sinusoid Equation1 has three parameters: Amplitude ($\boldsymbol{A}$), Frequency ($\boldsymbol{\omega} = \boldsymbol{2\pi f}$), and phase ($\boldsymbol{\varphi}$). (Lathi, 1995)

$$\boldsymbol{C(t) = A\,sin(2\pi f t + \varphi)} \qquad \textbf{(1)}$$

Using a binary stream of bits as a source signal S(t) to modulate one of the carrier parameters produces:

- BASK (Binary Amplitude Shift keying), by changing carrier amplitude according to Equation2

$$\boldsymbol{A(t) = \begin{cases} A & S(t) = 1 \\ 0 & S(t) = 0 \end{cases}} \qquad \textbf{(2)}$$

- BFSK (Binary Frequency Shift keying), use to different frequencies one for each bit value according to Equation3

$$\boldsymbol{f(t) = \begin{cases} f_1 & S(t) = 1 \\ f_0 & S(t) = 0 \end{cases}, f_1 > f_0} \qquad \textbf{(3)}$$

- BPSK (Binary Phase Shift keying), shifts the carrier by 180° for one of the bit values, i.e. (1) and don't shift it for the other bit value, i.e. (0) or vice versa which according to Equation.4

$$\boldsymbol{\varphi(t) = \begin{cases} 180° & S(t) = 1 \\ 0° & S(t) = 0 \end{cases}} \qquad \textbf{(4)}$$

All mentioned modulation schemes are illustrated in Figure.1

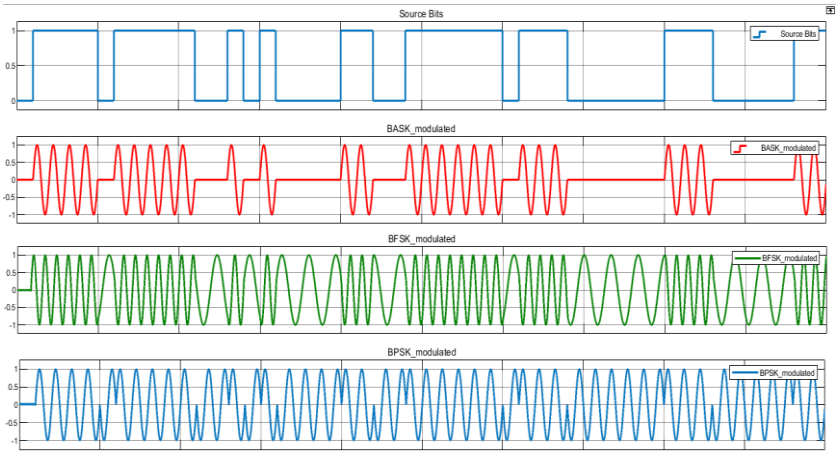

Figure 1 Basic modulation schemes illustration.

1.2. Research Problem:

The importance of developing a communication system has become a necessity and a prerequisite for contemporary life. a communication system has evolved in the last century from analog systems to digital systems to improve their performance and get rid of the noise problem, in addition of reducing the effect of distortion as much as possible. To accomplish this, signals whose values can be predicted should be used, even if they are affected by channel influences. One of these communication systems is the binary digital modulator (BDM) which refers to a kind of modulation that represents each binary symbol (M = 2) by one bit of information (N = 0 or 1), which is the information signal (message) to modulate a carrier signal by varying its amplitude, frequency, or phase. All these schemes are the digital implementation of the legacy analog communication systems. This analogy is as follows:

- Amplitude Modulation (AM) Amplitude Shift Keying (ASK)
- Frequency Modulation (FM) Frequency Shift Keying (FSK)
- Phase Modulation (PM) Phase Shift Keying (PSK)

This study is about how to derive a modified basic scheme circuits of modulation (Amplitude, Frequency, Phase) using digital programmable CMOS in simulation software (PSpice). Digital modulation in communication systems is presented in this research. Using digitally programmable CMOS with a DVCC, will help us understand how to add (CMOS) integrated circuits in basic schemes modulation circuits (amplitude modulation (AM), frequency modulation (FM), and phase modulation (PM)), In addition, it will guide us on how to program a digitally programmable CMOS on PSpice software.

1.3. Research Objectives:

This study aims to develop communication devices in general and modulation in particular. The research also aims to:

- Developing a digital modulation system using a new technology and idea, which is the digitally programmable CMOS (Complementary metal–oxide–semiconductor).
- Integrate the CMOS DVCC circuit as a modulator in the communication systems, as will be explained in chapter 3.
- Finally, simulate this new idea in communication by using a simulation program, which is PSpice software, and analyzing the results.

1.4. Importance of the Research

The importance of this study is concentrated on several points, the most important of which are:

- How to integrate and add a digitally programmable CMOS DVCC circuit instead of traditional modulation circuits if they are not available.
- The programming of digitally programmable CMOS that obtains more accurate results of modulation of a signal in amplitude, frequency, and phase modulation.
- A digital modulator using digitally programmable CMOS DVCC can control more wanted output waveforms and simulate them by using PSpice software. As will be explained and proved in this research.

1.5. Research Methodology:

This study adopts an applied research approach, focusing on how to integrate digitally programmable CMOS DVCC into communication systems as a digital modulator of a signal. And how to design and simulate this circuit to show the desired result. For that, this study analyzes the results by using one or more simulation software, for example, Matlab, Proteus, and PSpice.

Based on this methodology which shows the modulation of the signal in three-way of modulation:

- Amplitude Modulation (AM)
- Frequency Modulation (FM)
- Phase Modulation (PM)

And after merging a digitally programmable CMOS DVCC:

- DP ASK-Digitally programmable Amplitude shift keying,

- DP PSK-Digitally programmable Phase shift keying,
- DP FSK-Digitally programmable Frequency shift keying,

2. Literature review

This chapter includes the literatures and the previous studies that studied the variables of the current study as the following.

Realized that digitally programmable floating impedance converter electrical circuits based on two digitally programmable differential voltage current conveyors CMOS devices and grounded passive elements that can convert the thermal obstruction transformer to digital programmable floating arrestors such as the ideal floating resistor, capacitors, inductors, and passive resistors depending on the frequency by appropriate selection of three grounded elements without any component matching restrictions, the digitally programmable float transducer is therefore designed and verified based on PSPICE (Nahhas, 2013).

Depending on the first order modulators in sigma delta modulators oversampled analog to digital converters based on two phase latch comparators with the three stages in order to get 2500 DC, while floating gate named MOSFET is used at the input of integrator and comparators, and then the ADC is implemented through the 0.25 µm CMOS technology at the 205 Volt (Gandewar, Soni, & Sharma, 2016).

Presented CMOS the low voltage, low power, and with positive second generation current conveyors which called (CC II +) which use two n-channels differential pairs as a replacement of the complementary differential pairs which are represented in n-channels and p-channels in order to realize the stages' input, which contribute in allowing the rail to rail input and output operations which reduce the required current mirror number in the input stage. (CC II +) requires a voltage supply of ± 0.75 volt and a total standby current of 133 micro Amber. It can be said that the proposed (CC II +) is to realize CMOS through the second order maximally flat low pass filter, depending on the P Spice simulation results (Madian, Mahmoud, & Soliman, 2006).

Provides an overview about the ΣΔ modulation techniques for the effective and efficient implementation of analog and digital interfaces in the internet of things devices, which identify the main challenges of the designs can be derived from their integration in the deep nanometer CMOS and discuss the circuits and systems solutions, and it can be considered that the diverse application scenarios range from the ultra-low power into ultra-wide band of wireless communications (de la Rosa, 2017).

Proposed a new compact CMOS realization of the current mode of the first order all pass filter without depending on the external resistors, where the circuit can be created through ten transistors and only one external capacitor using number of transistors lower than the previously reported CM APFs depending on the active building block which called ABB approach; the CM APFs can be designed by 512 kHz pole frequency in typical process at 27 ^{o} C and it can be designed in 40 nm CMOS technology and validated by the SPICE simulations (Lahiri, 2011).

Provided a thesis about the adjustment of electronic oscillators which must be suitable for signal generation and study the nonlinear properties associated with the active elements considering its capability to in order to convert harmonic signal into chaotic wave form, where the thesis provide a model for real physical systems exhibiting chaotic behavior through depending on analog electronic building blocks in addition to modern functional devices such as (OTA, MO-OTA, CC II ±, DVCC ± and other devices) with the presentation of the experimental verification of the proposed structures, where one part of these deals with all available possibilities in analog digital synthesis of non-linear dynamic systems where the changes that occur in mathematical models and corresponding solutions. Finally, there are detailed analysis of the impact of the active elements practices in the terms of qualitative changes in global dynamic behaviors of the individual systems and the possible occurrence of the disorder destruction through parasitic properties of the dependable devices (Hruboš, 2016).

Described the physical constraints of ever shrinking CMOS transistors reacts very fast and consider a rapidly approaching atomistic from limits of mechanical limits, so the research aims to measure the probable development of the nanoscale devices which may work with effectiveness less than 10 nm, this can be coupled with the fact that the recent designs can be changed from the analog signal processing towards the current mode circuits which provide lower voltage swings, higher bandwidth and better signal linearity than the current system to the digitally controlled system which is the DVCC has been realized and conducted by the CNFETs with a similar CMOS circuit with 32 nm. The results show that the CMOS transistors requires about 418.6 µW, while the CNFET based system requires about 352.1 µW (Tripathi, Ansari, & Joshi, 2018).

Provided a new realization of the electronically controlled positive and negative floating capacitors multipliers which can be expressed through (C ±). The peculiarity of topology implements a floating equivalent capacitor between two of its input terminals than the grounded one.

The aim of this is to achieve the best performance which can be achieved by using the advantages provided by the current conveyor. This requires the resistor free and employs one dual-output second generation voltage conveyers which can be expressed in (VCII ±) with one electronically tunable differential voltage current conveyor (E-DVCC). This can be represented in (ABBs) active building blocks with one single grounded capacitor. The value of the simulated capacitors can be controlled by the means voltage control, which is used in the current gain control process between X and Z terminals of E-DVCC (Ferri, Safari, Barile, Scarsella, & Stornelli, 2022).

Presented a new wide band first order voltage mode which achieves a flat group delay about 60 PS with a pole/ zero pair located at about 4.5 GHz. The proposed circuit shows that there is a high linearity with consumption of 16 mw power. The results of the performed simulation refer to compression point which has the capability of the first order all pass filter and by this, converting first order all pass filter can be converted into second order all pass filter plus a grounded capacitor in order to demonstrate the proposed system (all pass filter) simulation results are conducted depending on Virtuoso Cadence in TSMC 180 nm CMOS processes (Aghazadeh, Martínez García, Saberkari, & Alarcón Cot, 2018).

Presented a digitally reconfigurable CNFET which is based on biquadratic multi-functional filter with the employment of DVCC at 32 nm. The CNFET: carbon nanotube field effect transistors can be considered to be the potential candidates in order to overcome the shortcomings with the scale of the CMOS transistors. The circuit utilizes single CNFET based DVCC block analog with the suitable arrangement of resistors and capacitors. The digital proposed reconfigurable multi-functional filter circuit was found to be able to obtain the programmable low, high or band pass filter configuration depending on the same topology (Chandra, Gupta, & Imran, 2021).

Provided a digitally controlled outputs biquadratic filter which utilizes two DVCC by its role as the active elements and the passive elements with the DVCC which considered to be 3 grounded resistors and 2 grounded capacitors which result a successful realized digitally controlled low pass and band pass filter responses and according to all this the current summing networks which are employed in the internal circuits of DVCC incorporates the digital control in the whole system where the whole system is tuned of cut off frequency through 3 bit digital control word. The circuit has been simulated using 0.25 micro TSMC parameters with PSPICE

in order to validate the theoretically analyzed results that have been conducted from the whole system (Arif & Ismail, 2014).

Focused on the design of the current mode instrumentation amplifiers for the portable implantable electrocardiography and for the applications of the electroencephalography. Because of the great importance of the of the current mode instrumentation amplifiers, there is a great attention in the medical instrumentation and read out circuits in the bio sensors. CMOS differential voltage of second-generation current conveyor (DVCC II) is based on the linear transconductance. The new band-pass instrumentation amplifier which is based on the DVSS II which is implemented also in the study with the concept of the proposed DVCC and instrumentation amplifier is validated numerically and the predicted performance which results 0.18 µm TSMC CMOS technology in the past layout simulation level depending on tool of Virtuoso with about ± 0.9 V of power supply, and it was found that the demonstrated design DVCC II has a wide dynamic range of about ± 400 m V and about ± 0.85 m A with power consumption of 148 µW. moreover, the proposed design of DVCC II provides different benefits from the good linearity over a wide range input signals and it also provides low input impedance at the terminal X (Karami Horestani, Karami Horastani, & Björsell, 2022).

Proposed filter brings significant reduction of the complexity in the comparison to the available fully differential or P-D filter topology. The first integer and fractional order of the differential voltage mode all pass filter (APF) which employs single differential voltage current conveyor (DVCC) by using one resistor and one grounded capacitor. The study found that the fractional order capacitor is dependable and can be used in gain response compensation of the proposed all pass filter, while the theoretical results show that the 0.8^{th} and 1^{st} order of all pass filter can be verified through the simulations of cadence spectre using the new structures of DVCC with TSMC 0.18 µm, while the CMOS process parameters are supplied with about ± 0.9 V (Herencsar, Sotner, Kartci, & Vrba, 2018).

Found that the DVCC is used to realize a multiple input and single output filter with the band pass with low pass characteristics depending on PSPICE simulations of the proposed system of DVCC with its based filter which are provided using 0.18 µm CMOS technology from the TMSC MOSIS and dual supply voltages of ± 0.6 V. The implementation of CMOS of DVCC that based on the operational transconductance amplifier with wide linear range. It is known that the fully differential signal processing has more advantages than the applications of the single ended signal processing (Shaktour, 2018).

Provided a new fully differential configuration containing first order low pass filter, high pass filter and all pass filter all together within the design of the same circuit, therefore the proposed fully differential configuration is simple and the one multiply output current differencing transconductance amplifier with one grounded capacitor. The design of the circuit includes a wide operating frequency range that reach 73 MHz, where the additional features the design depend on by the proposed circuits include using the lowest active and passive component numbers in addition to the following components as the suitability of the integrated circuit chip, support of the cascadability, electronic tenability, non-passive components matching restriction, response's ability of all first order low pass filter and high pass filter. Moreover, the cascading feasibility can be demonstrated through realizing a fully differential order low pass filter (Kumar, Kumar, Elkamchouchi, & Urooj, 2022).

Presented a reconfigurable fully all pass filter depended on CMOS – DVCC, so the study propose a topology that sues two DVCC analog with two resistors and two capacitors as well where the proposed system can control the phase angle of the realized fully differential all pass filter by the n-bit digital control word, and therefore the proposed topology of the filter gives an increase immunity to the external noise reduction even order the harmonics, the high resolution capability and configurability, finally it is a must to mention that the proposed filter circuit is simulated through the PSPICE where the results justify the theory (Khan, Masud, & Moiz, 2015).

Presented a design of voltage mode with three input single output multifunction for first order filter employing commercially available LT 1228 IC in order to provide easy verification for the proposed circuit depending on the laboratory measurements, so the proposed filter is considered to be very simple as it consists of a single LT 1228 as an active device including two resistors with one capacitor only, and according to this the output voltage node is low impedance results in easy cascade ability with other voltage configuration mode. The results show that the proposed filter provides about four responses of the filter which are low pass filter, high pass filter, inverting all pass filter and non-inverting all pass filter in one configuration of circuit. The results also show that the selection of the output filter responses is conducted without any additional inverting or double gains which is easy controlled through the digital applied method, while the pole frequency control and the phase responses are conducted by electronic way which named bias current. The performance of the proposed filter was simulated by a ± 5 V voltage

supply for all pass experimental results that lead to phase response for 1 kHz to 1 MHz frequency that changed from 180 degrees to zero degree (Jaikla et al., 2021).

Aimed to achieve the effective design of the analog and digital domains, where among all analog circuits, the multifunctional filter analog with multi-phase oscillator makes a building block of the critical importance. According to all this, the study aims to present a digitally reconfigurable with multi- input and multi-output voltage mode. The circuit comprises two differential voltage current conveyors (DVCC) with two grounded capacitors and two floating resistors where the digital controllability with current summing network is used. The quality factor can be achieved by the use of 3-bit digital control word while keeping constant frequency through the dependence on TSMC simulations of 0.25 µ m CMOS technology that performed in order to achieve the validate of theoretical prediction results (Imran, Arora, & Kumar, 2014).

Presented single input with multi output voltage mode universal biquadratic, where the proposed circuit incorporate digital programmability which depend on plus three type of differential voltage current conveyors (DVCC) with two grounded capacitors and three resistors, accordingly the circuits exhibit high input impedance realizes all standard filter's function that have the orthogonal control of the cut off frequency and for the required quality factor. The tenability parameters can be achieved by using a 3-bit digital control word, where the proposed circuit is amenable for the monolithic integration through the virtue of the fact that basically depend on the grounded capacitors. The results show that the circuit simulation can be achieved through PSPICE which are perfect with the theoretically predicted results (Khan & Ansari, 2012).

Presented CMOS differential voltage current conveyer based on the wide linear range trans conductor with the common mode detection where the DVCC exhibits wide dynamic input range with about ± 0.9 V. This is used in order to realize instrumentation amplifier, multiple input, single output filter and single input multiple output with universal filter which are simulated by PSPICE at the input of the integrator and the comparator using the technology of 0.25 µ m CMOS at 2.5 V. Accordingly the sigma delta modulator uses the first order modulator in order to convert the analog to digital for making the comparison with the pseudo two phase with the three stages cascading in order to get about 2500 DC gain depending on the floating gate (Hassan & Mahmoud, 2010).

Provided the instrumentation amplifier which exhibits the possible modes specifically voltage, current transadmittance and transimpedence modes by using the single differential voltage current conveyor (DVCC) with few active resistors. The proposed design provides different advantages such as high range of 3 DB frequency for both differential gain and common mode of rejection ratio, where the proposed topology of the different instrumentation amplifier are analyzed and simulated using 0.18 µm CMOS technology for the applied realization of the DVCC. The experimental verification using the commercially feedback operational amplifier is depended on to make the required check for practical feasibility of the proposed design (Vista, Pheiroijam, Pamu, Tarunkumar, & Ranjan, 2022).

Used eight oscillator circuits with two output current conveyors from the second generation which use grounded passive elements by its role with an independent control on the condition of the oscillators and on its frequency with new six oscillators and eight oscillators circuits using the differential current conveyors (DVCC). The eight DVSS oscillators are the base joints of the two output CC II oscillators (Soliman, 2012).

Provided the new first order voltage mode filter. The minimum active and passive components, as the proposed configuration depends basically on one differential voltage current conveyor, one grounded capacitor and one resistor. The results of the study show that there are several advantages of the applied system such as the dependence on only one current conveyor, the good performance on one grounded capacitor, the good employment on only one resistor, the good simulation realization of the first order (low pass, high pass and all pass) voltage mode from the same configuration, no need to impose component choice conditions and finally the low active and low passive of sensitivity performance. The HSPICE simulation results with TSMC 0.18 µm 1P6M CMOS process technology with ± 0.9 V voltages supply; it was found that the proposed system achieves and validate the theoretical predictions (Chen, Huang, & Huang, 2012).

Proposed a new method of bandgap voltage reference circuit which designed using CMOS differential voltage current conveyor, where the proposed circuit depends on single DVCC for reducing the devices' number used in bandgap core and to start up circuit. Through the simulation of the study, it was found that the voltage of 500 MV, the temperature coefficient of 20 ppm /^{o}C which is successfully operated using the minimum supply voltage of 1.2 V in a range of temperature of 0-100 ^{o}C and with a total power dissipation of 56.6 µW at the room temperature (Hongprasit, 2014).

3. Simulation and Analysis

3.1- DVCC Module

A CMOS differential voltage second generation current conveyor (DVCCII) is offered. Wide bandwidth, low voltage operation, low input impedance at the X-terminal, and low offset voltage at the X-terminal are some of DVCCII's benefits. It is a helpful set of building blocks for analog circuits, particularly in situations when differential input is required. It can be utilized directly to construct necessary analog functions using MOS transistors operating in the ohmic region. PSPICE simulations show that the proposed DVCCII performs extremely well (Senani, Bhaskar, & Singh, 2015).

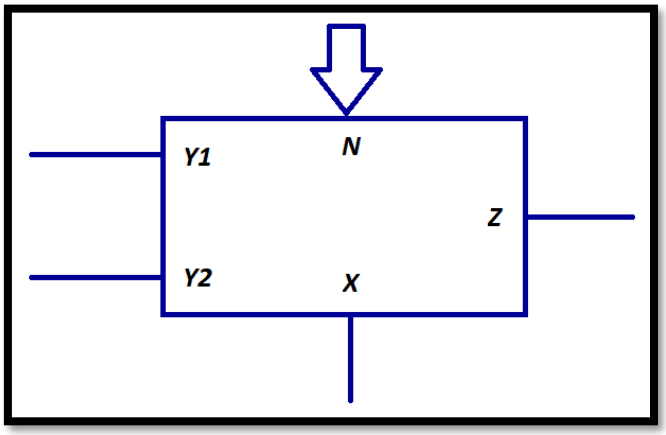

Figure 2. Differential Voltage Current Conveyor (DVCC) module.

A DVCC which shown in figure2 is a versatile module with two main voltage inputs V_{y1}, V_{y2} and a control input through current I_x, and a digital word which specify the output current I_z gain as multiples of the input current I_x. while the control terminal voltage V_x, and output voltage V_z both equals to the difference between the two input voltages V_{y1}, V_{y2}. [26]

The complete system input output characteristics is specified by the matrix in Equation5

$$\begin{bmatrix} I_{y_1} \\ I_{y_2} \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & k & 0 \end{bmatrix} \begin{bmatrix} V_{y_1} \\ V_{y_2} \\ I_x \\ V_z \end{bmatrix} \qquad (5)$$

The digital control word N consists of four bits [b_0 b_1 b_2 b_3] and calculates the current gain k according to Equation.6 if all output branches transistors aspect ratio is the same.

$$k = \frac{I_z}{I_x} = \sum_{i=0}^{3} b_i \times 2^i \qquad (6)$$

In case of different branches transistors aspect ratios (NMOS and PMOS transistors) Which are given by Equation.7 becomes the reference and k will be the decimal value of the binary word $[b_3\ b_2\ b_1\ b_0]_2$

$$\left(\frac{W}{L}\right)_i = 2^i \left(\frac{W}{L}\right)_{12} \qquad (7)$$

3.2 CMOS DVCC Circuit Implementation

On a micro scale the circuit schematic diagram in figure3 shows the CMOS realization of the DVCC, which consists of 26 MOSFETs its operation is as follows:

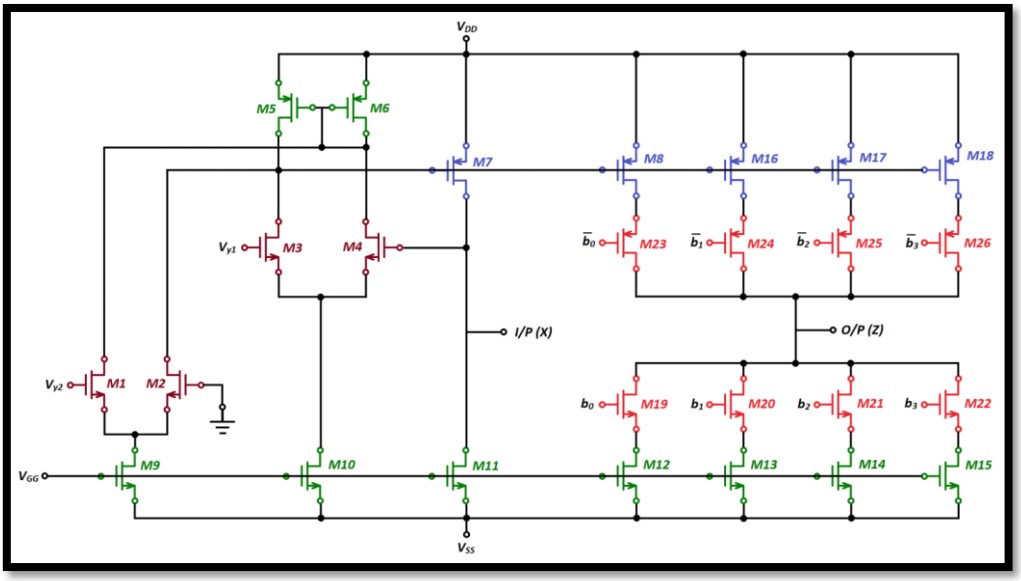

Figure 3 CMOS realization of the DVCC.

- M_1 & M_2 forms a differential pair that works in single ended mode where the input voltage V_{y2} controlling M_1 Gate terminal, while Gate terminal of M_2 is grounded.
- M_3 & M_4 are connected in parallel with M_1 & M_2 forming another differential pair that works in double ended mode with inputs V_{y1} & V_x.
- M_5 & M_6 works as an active load for both differential pairs, also they work as a current mirror to assure the current symmetry in differential pair arms.
- M_9 & M_{10} are the active source resistance R_s of the differential pairs determine the source current I_s and the DC operating point 'Q-point' by voltage V_{BB}.

- M_7 & M_{11} work as a common source amplifier its input is the common output of the differential pairs from M_1 & M_2. M_{11} is the drain active load of the amplifier R_D. the amplifier output is also the input terminal X is connected to M_4 as a feedback to determine the double ended differential pair input with V_{y1}.
- M_8, M_{16}, M_{17}, & M_{18} each works as a common source amplifier their drain loads is M_{12}, M_{13}, M_{14}, & M_{15} respectively.
- M_{19} : M_{26} are just switches connect or disconnect their branches to the output terminal Z to increase the output current as mentioned before.

And CMOS DVCC circuit that was implemented on PSpice is showed in figure4

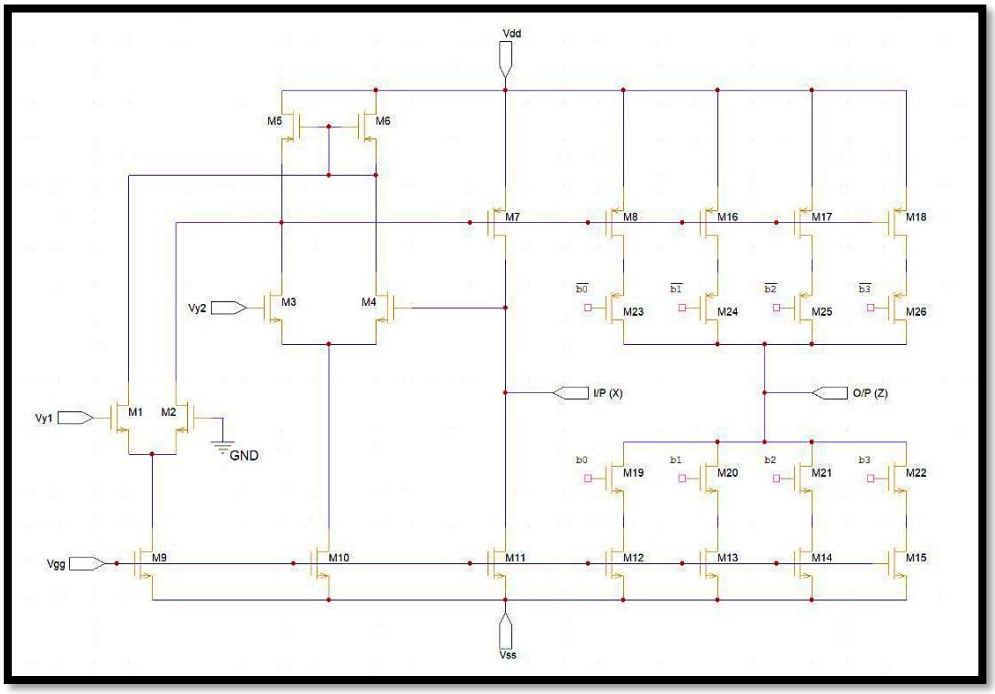

Figure 4 CMOS implementation for DVCC in PSpice.

3.3. Simulation Result

The main idea in this thesis is to design a current controlled digital programable modulator using CMOS gates and DVCC modules as follows:

3.3.1. DP BASK_Digitally programmable Binary Amplitude shift keying:

Figure5 shows the design of a binary amplitude shift keying modulator. Which consists of a DVCC with sinusoidal input ***C(t)*** controlled by a source digital binary data ***S(t)*** through NMOS transistor working as a switch. The input and output waveforms are shown on the same figure also.

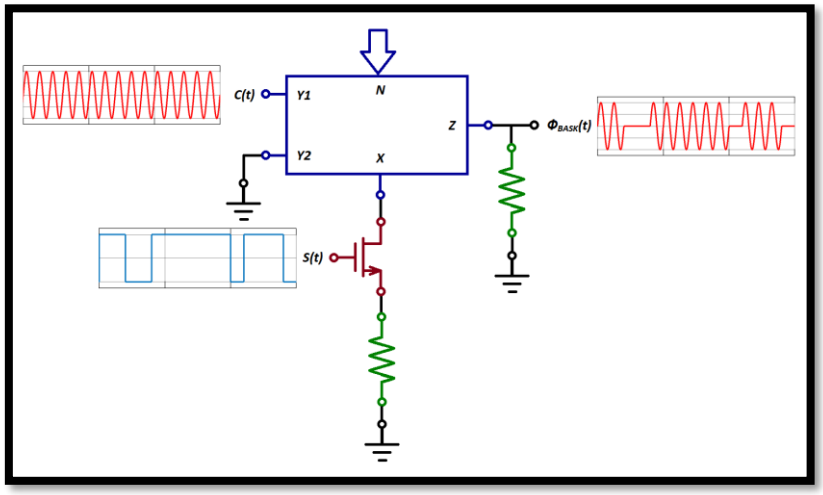

Figure 5 DP-BASK scheme.

3.3.2. DP BPSK Digitally programmable Binary Phase shift keying:

This modulator uses two DVCCs working in single ended mode with the same carrier input ***C(t)*** but in different inputs to create a phase inverted signal ***-C(t)*** from lower DVCC. The source bits ***S(t)*** used with a CMOS inverter to drive the DVCCs. 1's will pullup making output equals to ***C(t)***, while 0's will pulldown making output equals ***-C(t)***. Figure6 shows the schematic and waveforms.

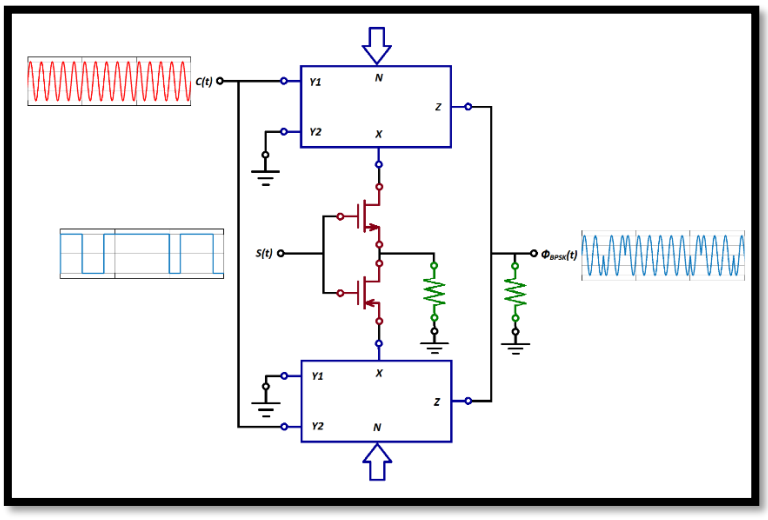

Figure 6: DP-BPSK scheme.

3.3.3. DP BFSK Digitally programmable Binary Frequency shift keying:

The last scheme shown in Figure7 is the BFSK scheme, using two DVCCs each with a different input frequency $C_0(t)$, and $C_1(t)$. the driver is also a CMOS inverter when input signal ***S(t)*** equals 1 the inverter pullup making the output equals to $C_1(t)$, and $C_0(t)$ for the pulldown state. All waveforms are shown in the same figure.

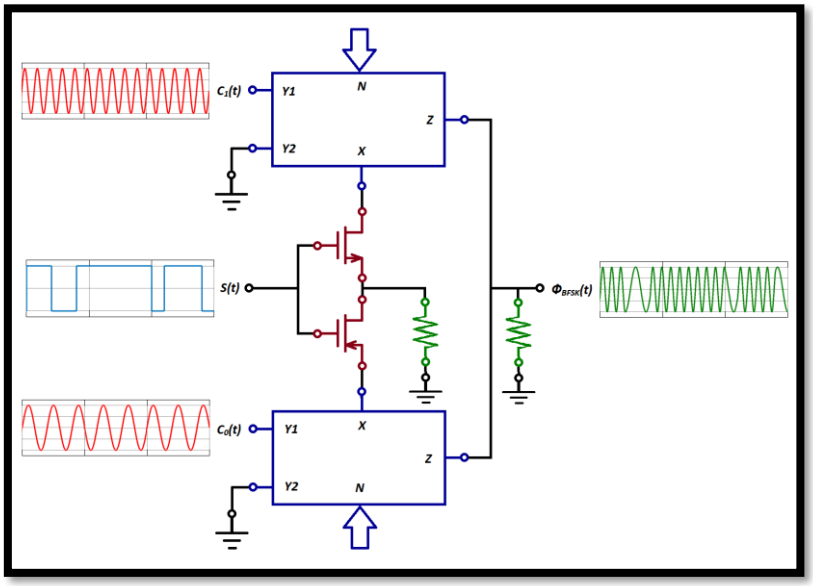

Figure 7: DP-BFSK scheme.

4. Conclusion:

Simply put, modulation is a common practice in communication systems where a very high-frequency carrier wave is used to transmit a low-frequency message signal, preserving all the information available in the original message signal. After this modulation process, the demodulation process is used to separate the original information from the modulated carrier. The modulation process, particularly digital modulation, is the focus of this study.

To enhance performance, eliminate the noise issue, and minimize the distortion effect, communication systems have evolved over the past century from analog systems to digital systems. Digital modulation is the latest way in wireless communications. It includes several methods for modulating the carrier signal using the source signal. Specifically, by including the digital signal in one of the characteristics of the carrier signal (amplitude, frequency, or phase). This way of sending the digital information implicitly in the analog signal (the carrier signal). Additionally, during the modulation process, the carrier signal's amplitude, frequency, or phase can change depending on the input data. These are the simplest methods of digital modulation, of course, there are more complex methods that exist by mixing the previous methods.

In this study, the three straightforward techniques for digital modulation were reviewed while they were being enhanced and made more effective. using the Complementary Metal Oxide Semiconductor (CMOS) technique, Amplitude Shift Keying (ASK), Frequency Shift Keying (FSK), and Phase Shifting Keying (PSK), all these methods were simulated by using MATLAB, and PSpice software.

5. Results:

- The study demonstrated that the CMOS DVCC circuit could be successfully integrated into communication systems as a digital modulator.
- The introduction of digitally programmable modulation techniques, specifically DP BASK, DP BPSK, and DP BFSK, showed significant improvements in signal processing. The simulation results indicated that these techniques provided better control over signal modulation compared to traditional methods, leading to more efficient communication systems.
- The use of PSpice and MATLAB for simulation validated the effectiveness of the digitally programmable CMOS technology. The simulation results closely matched the expected outcomes, confirming the theoretical models developed in the study.
- The study found that the use of digitally programmable modulation techniques reduced signal distortion and interference, leading to improved signal integrity.

6. Recommendations:

- The study recommended to conduct further research on the noise resistance capabilities of the DP modulation techniques.
- Explore additional modulation techniques that could benefit from digitally programmable CMOS technology, such as Quadrature Amplitude Modulation (QAM) or Orthogonal Frequency-Division Multiplexing (OFDM).
- Focus on optimizing the power consumption of the digitally programmable CMOS circuits. As communication systems increasingly demand energy efficiency.

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8. Appendix

List of Abbreviations:

Abbreviations	*Description*
CCI	First Generation Current Conveyor
CCII	Second Generation Current Conveyor
DP	Digitally Programmable
CMOS	Complementary Metal-Oxide-Semiconductor
DVCC	Differential Voltage Current Conveyor
BDM	Binary Digital Modulator
AM	Amplitude Modulation
PM	Phase Modulation
FM	Frequency Modulation
ASK	Amplitude Shift Keying
PSK	Phase Shift Keying
FSK	Frequency Shift Keying
MISO	Multiple Input Single Output Level
SIMO	Single Input Multiple Output Level

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